ABSTRACT

An pipeline analog-to-digital converter (ADC) is provided that is capable of applying calibration at a resolution greater than the resolution of a digital output signal provided by the ADC. The ADC includes a calibration component adapted to apply calibration bits to digital output bits generated by stages of the pipeline and corresponding to samples of an analog input signal. The ADC also includes a random number generator that provides at least one random bit having a sub-LSB bit weight. The calibration bits and the at least one random bit are applied as a dither to the digital output bits such that, on average, the digital output signal provided by the ADC is calibrated at a sub-LSB resolution.